Effect of heat and Mechanical Properties on Thermal Vias of PCB Mounted Driven of QFN Package

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Introduction

The semiconductor and IC package manufacturer are continuously seeking for miniaturization devices to fix into a small space. An unfortunate miniaturization of devices will have an effect on heat dissipation density, which leads to low rate of heat dissipation to the ambient. As a result, the chip temperature increases which eventually degrade the entire system of the circuit. Besides that, the relationship between temperature and functioning of electronic device is well known. When the devices keep running somehow will increases the junction temperature. This junction temperature is due to internal self-heating which is a byproduct of electrical current flow in the electronic device during operation. Increasing the junction temperature will degrade performance of the electronic device beside that physical defect will occur. Therefore, the benefit of miniaturization device can be easily lost if the thermal management is not made properly.
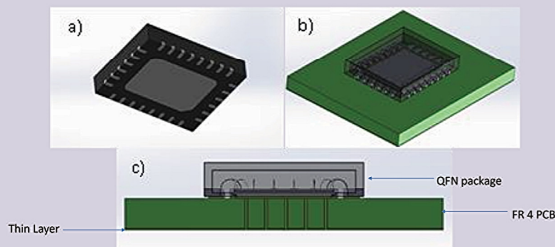
Specification of Model and Boundary

Fig1. a) QFN package, b) QFN package mounted on PCB, and c) Thermal vias on PCB

As shown in figure 1, the dimension of QFN package is 4x5x0.9mm, it consist of Molded compound, silicon die, die attached material, lead, and exposed paddle.

Figure 1 also depict thermal vias on PCB, the dimension of PCB is 25x25x0.8mm. Beside that, vias is coated by copper with 1oz thickness.

Materials	Thermal Conductivity (W/mK)	Thermal Capacity (J/Kg K)	Density (Kg/m3)
Epoxy Mold Compound	0.72	794	2020
Silicon (25C)	148	712	2328.9
SnPb Solder	50	150	8500
Silver Filled Die Attach	2.09	714	3560
FR-4	0.35	878.6	1938

Computational Method

➢ Heat transfer module.
➢ QFN package mounted on the PCB is designed with Solidworks and imported to COMSOL Multiphysics 5.1 using Livelink.
➢ Thin layer is applied to copper thin film
➢ Heat Source is given to the Die of the IC
   Q=0.55

Results

The higher thermal resistance from junction to ambient (θja) the higher temperature of IC package for a given amount of heat dissipation. Therefore, a higher θja value leads to higher junction temperature for a given amount of heat dissipation.

The obtained thermal resistance result from the simulation were calculated by using:

$$R=\theta/Q$$

Where θ is the temperature excess of heat source area obtained by simulation, Q is heat rate input in the simulation.
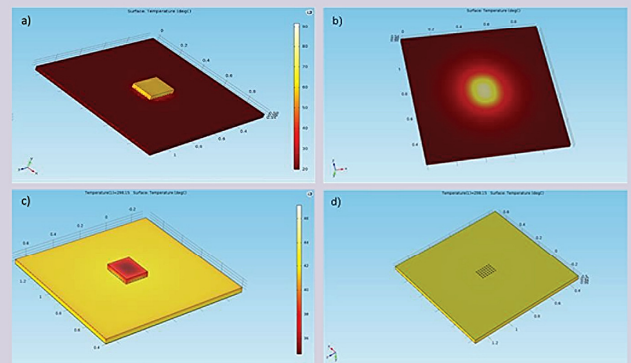

Fig2. Heat Contribution from QFN package into a) PCB without vias at front dide, b) PCB without vias at back side c) PCB with vias at front side, and d) PCB with vias at back side

Test Board	PCB- FR4	PCB-FR4 with copper vias
Thickness (mm)	0.8	0.035
Width (mm)	25	25
Length (mm)	25	25
Thermal resistance θja (°C/W)	140	43

Conclusion

The influence of the thermal via configuration, will increase the amount of the heat transfer. Therefore, the functionality of the IC driver will be efficient as the operating temperature is maintained to be in the compatible range. The temperature distribution in the QFN package will give us the optimized design of the thermal vias and hence, an efficient driver configuration can be generated.

References

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2. Xiobing Luo, Zhangming Mao, Sheng Liu, "A thermal model for calculating thermal resistance of eccentric heat source on rectangular plate with convective cooling existing at upper and lower surfaces", IEEE, 2009.

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