$La_5Ca_9Cu_{24}O_{41}$ Layers as 1D Heat Spreaders for Thermal Management Solutions

Ch. Orfanidou[1] and J. Giapintzakis[1]
[1]Department of Mechanical and Manufacturing Engineering, University of Cyprus, Nicosia, Cyprus
*Corresponding author: 75 Kallipoleos Avenue P.O. Box 20537, Nicosia, 1678, Cyprus
email: orfanidou.charis@ucy.ac.cy

Abstract: This paper deals with the design of a viable thermal management solution using $La_5Ca_9Cu_{24}O_{41}$ layers for heat channeling. The simulations are carried out with the finite element method using COMSOL Multiphysics Heat Transfer Module [1]. COMSOL 4.2 was used to model and optimize silicon devices. Malfunctioning elements on silicon devices are sometimes converted into hotspots resulting in the increase of their temperature and that of the adjacent elements. The simulations carried out demonstrate a temperature decrease of the adjacent elements when $La_5Ca_9Cu_{24}O_{41}$ layers are introduced in such devices.

Keywords: Thermal management, 1D heat conduction, hot spot, silicon devices, $La_5Ca_9Cu_{24}O_{41}$ heat spreader

1. Introduction

The continuing miniaturization in semiconductor technology has led to nanoscale chip feature sizes and significant increases in on-chip power dissipation as well as heat flux at the silicon level [2]. At the same time, the desire for lower operating temperatures is compounding the thermal challenge. Materials and process improvements are required to minimize thermal resistance at the interfaces. The concurrent development and packaging of all these elements is critical to ensure that from a cost and availability perspective a viable thermal design solution exists.

Thermal management in innovative technology is a major problem to be solved, especially in novel electronic devices, such as further miniaturized microchips, hard disks and interfaces between biological structures and semiconductor microstructures.

The 1D Heisenberg antiferromagnet $La_5Ca_9Cu_{24}O_{41}$ exhibits highly anisotropic magnon-mediated thermal conductivity while at the same time is electrically insulating (see Fig. 1) [3]. In this work, we evaluate the feasibility of using $La_5Ca_9Cu_{24}O_{41}$ layers for thermal management solutions in electronic devices [4]. We simulate heat propagation in silicon structures with and without $La_5Ca_9Cu_{24}O_{41}$ layers. This approach is similar to that followed in [4] using graphene layers.

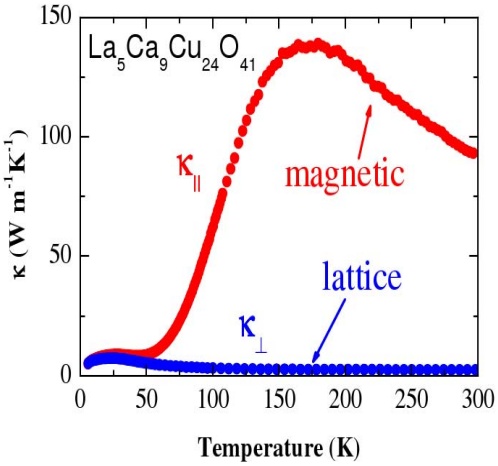

Figure 1. Thermal conductivity of the spin ladder material $La_5Ca_9Cu_{24}O_{41}$, measured parallel ($\kappa_{||}$) and perpendicular ($\kappa_{\perp}$) to the ladders [3].

2. Model of Heat Conduction – Governing Equations

We model a cross-section of a silicon device where we simulate 10 semiconductor transistors which generate heat as square operating elements, separated from each other by 1 μm (see Fig. 2). The forth operating element, counting from the left, plays the role of the hot spot as shown in Fig. 2. The thickness of the Si substrate is 500 μm and on top there is a 3.4 μm-thick rectangular layer which could be either $La_5Ca_9Cu_{24}O_{41}$ or silicon. The thermal conductivity of silicon is assigned to be 150 $W/(m\cdot K)^{-1}$ [5] and the thermal conductivity of the anisotropic $La_5Ca_9Cu_{24}O_{41}$ layer is {1, 1, 100} $W/(m\cdot K)^{-1}$ [3]. A conventional heat sink is attached to the bottom of device structure.

The heat conduction was modeled by solving numerically the steady state, two-dimensional heat conduction equation:

$$\frac{\partial}{\partial x}\left(\kappa\frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}\left(\kappa\frac{\partial T}{\partial y}\right)=0 \qquad (1)$$

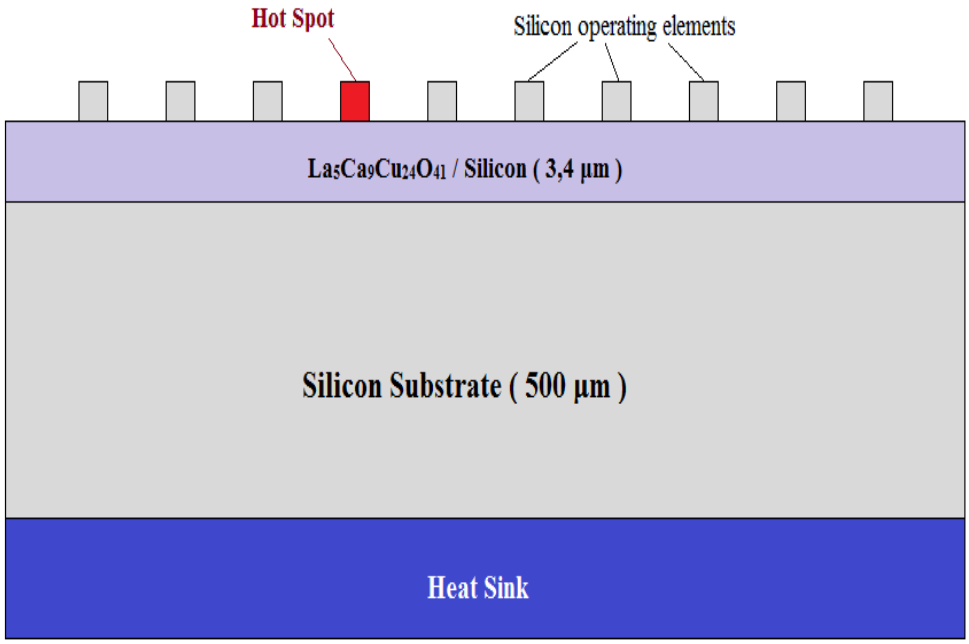

Figure 2. Schematic of the silicon device, showing where the additional $La_5Ca_9Cu_{24}O_{41}$ or silicon layer is introduced and also the heat sink which is placed at the bottom. The thicknesses are not to scale.

where T is the absolute temperature, and κ is the local value of thermal conductivity. A normal heat flux is applied at the top of the silicon operating elements using Fourier's law:

$$Q_y = -\kappa [\, \partial T / \partial y \,] \qquad (2)$$

where Q_y is the heat source, T is the absolute temperature, κ is the thermal conductivity and y is the distance along the thickness direction of the device. A value of 10^8 W/m^2 was used for the heat flux of the operating elements while for the hot spot element alone the heat flux was set to 10^{10} W/m^2. The internal boundaries between the components of the circuit were assumed to be thermally continuous. The bottom surface of the substrate was kept at a constant temperature T_0=300 K. The external surfaces were modeled as adiabatic or insulated from environment, i.e., the temperature gradients across these surfaces were set to zero. No convection was taken into account so that the maximum possible operating temperature was obtained.

The mesh used for the simulation was free triangular with a scale factor of 10x10 as shown in Fig. 3. The total number of the mesh elements is 3066 and each operating element (including the hot spot) consists of 4 mesh elements.

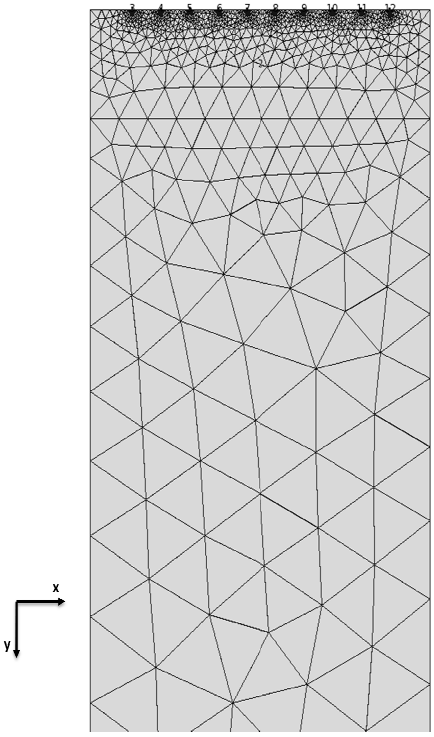

Figure 3. Schematic of the silicon device, showing the mesh used for the simulations presented. The device continues along the y direction.

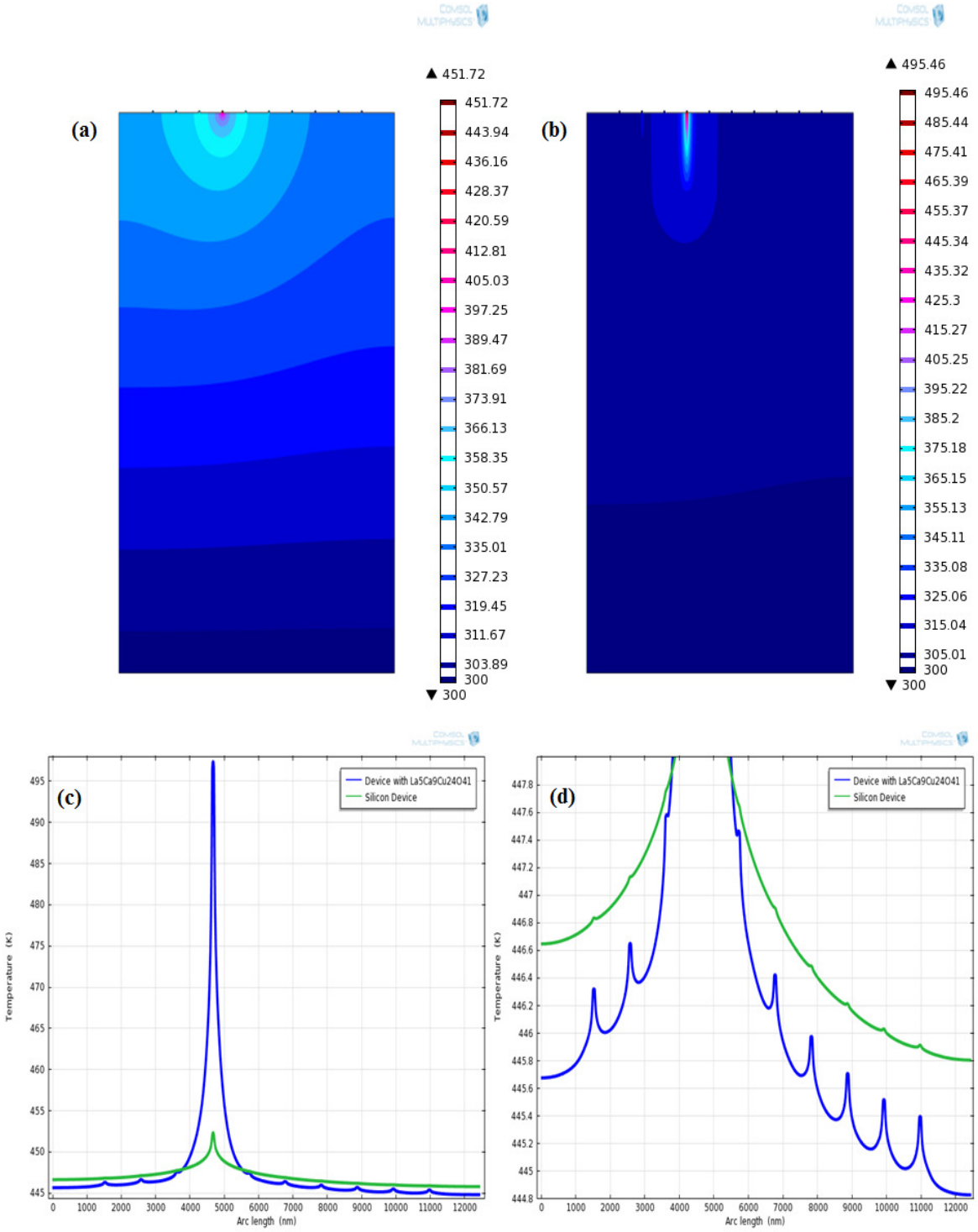

Figure 4. Plots (a) and (b) show the temperature distribution, contour: conductive heat flux, in (a) an all silicon device and (b) a silicon device with a $La_5Ca_9Cu_{24}O_{41}$ layer. Plots (c) and (d) show the temperature profiles along the surface located at the bottom of the operating elements. The blue line is the temperature profile of the device with the $La_5Ca_9Cu_{24}O_{41}$ layer and the green line of the device without the $La_5Ca_9Cu_{24}O_{41}$ layer. Plot (c) shows the entire temperature profile and plot (d) a zoom of this temperature profile of the nine (9) adjacent of the hot spot operating elements. Note that their temperature is lower in the case of incorporating the $La_5Ca_9Cu_{24}O_{41}$ layer.

3. Simulation Results

In Fig. 4 we demonstrate the results of the numerical studies that have been carried out. In plots (a) and (b) is shown the temperature distribution in the silicon devices without and with the $La_5Ca_9Cu_{24}O_{41}$ layer, respectively. We can obviously observe isotropic heat conduction in plot (a) and anisotropic heat conduction, or heat channeling, caused by the introduction of the $La_5Ca_9Cu_{24}O_{41}$ layer in plot (b).

In plot (c) the entire temperature profiles are shown. In the device without the $La_5Ca_9Cu_{24}O_{41}$ layer a high temperature is produced at the hot spot created because of the malfunctioning forth element. An even higher temperature is produced at the hot spot in the device with the $La_5Ca_9Cu_{24}O_{41}$ layer because of the thermal resistance due to the introduction of a different material in it. In plot (d) a close up of plot (c) is shown. By introducing the $La_5Ca_9Cu_{24}O_{41}$ layer we can keep the operating elements placed adjacent to the hot spot at lower temperature than without it. The temperature reduction obtained for this geometry varies from 0.2K to 1K. Thus while the thermal resistance in the device with the $La_5Ca_9Cu_{24}O_{41}$ layer results in an even higher hot spot temperature; nevertheless, the temperature of the adjacent operating elements is lower than in the device without the $La_5Ca_9Cu_{24}O_{41}$ layer.

In other numerical studies undertaken we have obtained temperature reduction of the adjacent operating elements from 1K to several degrees Kelvin, by changing parameters of the geometry of our device such as the $La_5Ca_9Cu_{24}O_{41}$ layer thickness, the distance between the operating elements and the silicon substrate thickness. In these studies we have observed that in the majority of the times we obtain lower operating temperatures with the incorporation of the $La_5Ca_9Cu_{24}O_{41}$ layer.

4. Conclusions

We carried out a feasibility study of using $La_5Ca_9Cu_{24}O_{41}$ layers as 1D heat spreaders in silicon devices. Incorporating $La_5Ca_9Cu_{24}O_{41}$ layers leads to a reduction of the temperature of the adjacent of a hot spot operating elements "protecting" them from the exceeding heat generating at the hot spot region of the chip. The efficiency of the hot spot heat removal with $La_5Ca_9Cu_{24}O_{41}$ layers depends on the specifics of the device structure and geometry. The numerical experiments realized give us encouraging results and we expect to verify them with the scheduled experimental studies. The developed model and obtained results are important for the design of 1D $La_5Ca_9Cu_{24}O_{41}$ heat spreaders for thermal management solutions, having in mind that the reduction of each temperature degree can increase significantly the lifetime of the semiconductor electronic devices.

5. References

1. [Online] Available: http://www.comsol.com
2. R. Viswanath et al., Thermal Performance Challenges from Silicon to Systems, *Intel Technology Journal*, **Quarter 3** (2000)
3. C. Hess et al., Magnon heat transport in (Sr, Ca, La)14Cu24O41, *Physical Review B*, **vol. 64**, 184305 (2001)
4. S. Subrina et al., Heat Removal in Silicon-on-Insulator Integrated Circuits with Graphene Lateral Heat Spreaders, *IEEE Electron Device Letters*, **vol. 30**, pp 1281-1283 (2009)
5. *American Institute of Physics Handbook*, 2nd edition, page **4**-93. McGraw-Hill Book Company (1963)

6. Acknowledgements

We would like to thank Prof. D. Grigoriadis for valuable discussions and suggestions. This work was supported by the European Commission through the ITN Marie Curie LOTHERM, Contract Number: PITN-GA-2009-238475.